WHAT IS CLAIMED IS:

1. A clock recovery circuit for recovery of a clock from an input signal digitalized, said clock being in synchronization with said input signal,

said clock recovery circuit comprising:

a clock generation part for generating a clock signal;

a phase error detection part for detecting a phase error of said input signal with respect to said clock signal; and

a control part for controlling, based on an output of said phase error detection part, an oscillation frequency of said clock generation part so that said phase error becomes zero;

said phase error detection part including:

a cross detection part for generating a timing signal representative of a point at which said input signal crosses a preset value;

a phase error estimation part for estimating, based on said timing signal, said phase error of said input signal with respect to said clock signal;

a pattern detection part for detecting a variation pattern of said input signal; and

a selection part for selecting, according to said detected variation pattern, whether said estimated phase error is output to said control part.

2. The clock recovery circuit of claim 1,

said pattern detection part including:

a hold part for holding said input signal as time series data;

a comparison part for comparing data items stored in said hold part with preset variation patterns; and

a logical circuit part for controlling, when it becomes clear from a result of said comparison that the variation pattern of said input signal indicates a specified pattern, said selection part so that said estimated phase error is not output to said control part.

3. The clock recovery circuit of claim 1,

said pattern detection part including:

a hold part for holding said input signal as time series data;

a comparison part for comparing in size at least two items of data stored in said hold part with preset threshold values; and

a logical circuit part for controlling, when it becomes clear from said at least two data items and from a result of said comparison that the variation pattern of said input signal indicates a specified pattern, said selection part so that said estimated phase error is not output to said control part.

4. The clock recovery circuit of claim 1,

said pattern detection part including:

a first hold part for holding said input signal as time series data;

a subtraction part for sequentially calculating a differential of two consecutive data items stored in said first hold part;

a second hold part for holding a serial output of said subtraction part as time series data; and

a logical circuit part for controlling, when it becomes clear from the serial output of said subtraction part and from at least one item of data stored in said second hold part that the variation pattern of said input signal indicates a specified pattern, said selection part so that said estimated phase error is not output to said control part.